ABSTRACT OF THE DISCLOSURE

A clock management scheme for an 802.11 MAC on a PCI or Cardbus bus that works in conjunction with industry standardized power mechanisms. The scheme involves enabling and disabling the main clock in coordination with IEEE 802.11 protocols and is compatible with ACPI power management and configuration interface specification. When the main clock is disabled the MAC and supporting hardware can run off either a lower frequency oscillator or the bus clock. The bus clock is automatically used when it is required by accesses by the host to the card.